

**Amendments to the Specification:**

Please replace the paragraph beginning at page 1, line 5, with the following rewritten paragraph:

This application relates to the following commonly assigned co-pending applications entitled:

~~"Scan Wheel—An Apparatus And Method For Interfacing A High Speed Scan-Path With A Slow-Speed Tester Equipment," Serial No. 09/653,642~~, filed August 31, 2000, Attorney Docket No. 1662-23700; ~~"Priority Rules For Reducing Network Message Routing Latency~~~~Rotary Rule And Coherence Dependence Priority Rule," Serial No. 09/652,322~~, filed August 31, 2000, Attorney Docket No. 1662-27300; ~~"Speculative Scalable Directory Based Cache Coherence Protocol," Serial No. 09/652,703~~, filed August 31, 2000, Attorney Docket No. 1662-27400; ~~"Scalable Efficient I/O Port Protocol," Serial No. 09/652,391~~, filed August 31, 2000, Attorney Docket No. 1662-27500; ~~"Efficient Translation Lookaside Buffer Miss Processing In Computer For Applications Using Large Pages In Systems With A Large Range Of Page Sizes By Eliminating Page Table Level," Serial No. 09/652,552~~, filed August 31, 2000, Attorney Docket No. 1662-27600; ~~"Fault Containment And Error Recovery Techniques In A Scalable Multiprocessor," Serial No. 09/651,949~~, filed August 31, 2000, Attorney Docket No. 1662-27700; ~~"Speculative Directory Writes In A Directory Based Cache Coherent [[-]]Non-Uniform Memory Access Protocol," Serial No. 09/652,834~~, filed August 31, 2000, Attorney Docket No. 1662-27800; ~~"Special Encoding Of Known Bad Data," Serial No. 09/652,314~~, filed August 31, 2000, Attorney Docket No. 1662-27900; ~~"Mechanism To Track Keep All Pages Open Pages In A DRAM Memory System," Serial No. 09/652,704~~, filed August 31, 2000, Attorney Docket No. 1662-28100; ~~"Programmable DRAM Address Mapping Mechanism," Serial No. 09/653,093~~, filed August 31, 2000, Attorney Docket No. 1662-28200; ~~"Computer Architecture And System For Efficient Management of Bi-Directional Bus~~~~Mechanism To Enforce Memory Read/Write Fairness, Avoid Tristate Bus Conflicts, And Maximize Memory Bandwidth," Serial No. 09/652,323~~,

filed August 31, 2000, Attorney Docket No. 1662-29200; "An Efficient Address Interleaving With Simultaneous Multiple Locality Options," Serial No. 09/652,452\_\_\_\_\_, filed August 31, 2000, Attorney Docket No. 1662-29300; "A High Performance Way Allocation Strategy For A Multi-Way Associative Cache System," Serial No. 09/653,092\_\_\_\_\_, filed August 31, 2000, Attorney Docket No. 1662-29400; "A Method And System For Absorbing Defects In Improving The Yield Of A High Performance PMicroprocessor With A Large On-Chip N-Way Set Associative Cache," Serial No. 09/651,948\_\_\_\_\_, filed August 31, 2000, Attorney Docket No. 1662-29500; "A Method For Reducing Directory Writes And Latency In A High Performance, Directory-Based, Coherency Protocol," Serial No. 09/652,324\_\_\_\_\_, filed August 31, 2000, Attorney Docket No. 1662-29600; "Mechanism To Reorder Memory Read And Write Transactions For Reduced Latency And Increased Bandwidth," Serial No. 09/653,094\_\_\_\_\_, filed August 31, 2000, Attorney Docket No. 1662-30800; "System For Minimizing Memory Look-Ahead Mechanism To Minimize And Manage Bank Conflicts In A Computer Memory System," Serial No. 09/652,325\_\_\_\_\_, filed August 31, 2000, Attorney Docket No. 1662-30900; "Computer Resource Management And Allocation SystemScheme That Ensures Forward Progress, Maximizes Utilization Of Available Buffers And Guarantees Minimum Request Rate," Serial No. 09/651,945\_\_\_\_\_, filed August 31, 2000, Attorney Docket No. 1662-31000; "Input Data Recovery Scheme," Serial No. 09/653,643\_\_\_\_\_, filed August 31, 2000, Attorney Docket No. 1662-31100; "Fast Lane Prefetching," Serial No. 09/652,451\_\_\_\_\_, filed August 31, 2000, Attorney Docket No. 1662-31200; "A Mechanism For Synchronizing Multiple Skewed Source-Synchronous Data Channels With Automatic Initialization Feature," Serial No. 09/652,480\_\_\_\_\_, filed August 31, 2000, Attorney Docket No. 1662-31300; "A Mechanism To Control The Allocation Of An N-Source Shared Buffer," Serial No. 09/651,924\_\_\_\_\_, filed August 31, 2000, Attorney Docket No. 1662-31400; and "Chaining Directory Reads And Writes To Reduce DRAM Bandwidth In A Directory Based CC-NUMA Protocol," Serial No. 09/652,315\_\_\_\_\_, filed August 31, 2000, Attorney Docket No. 1662-31500, all of which are incorporated by reference herein.